**CMPN103- Programming Techniques**

**Logic Simulator Project**

**Documentation**

***Submitted to:***

*Dr. Lydia Wahid*

*TA. Eman Hosam*

*TA. Youssef Ghatas*

*TA. Reem Elsayed*

***Team Members and ID:***

*Ahmed Mohamed Mohamed Abdulsalam 1190567*

*Ahmed Tarek Abdellatif AbdellHafiz 1190157*

*Joseph Ameer Aziz 1190052*

***Team Emails:***

- *ahmed.abdelssalam01@eng-st.cu.edu.eg*

*- joseph.aziz02@eng-st.cu.edu.eg*

**Workload Division**

|  |  |  |
| --- | --- | --- |
| **Name** | **ID** | **Workload** |
| Joseph Ameer Aziz | 1190052 | -Get String function in Input  -Add gates and its validation  -Some Validations over connections  -Add label and Edit  -Select in design and simulation.  -Simulate (Sorting) |
| Ahmed Tarek Abdellatif AbdellHafiz | 1190157 | -Most if not all of Phase I implementation:  including Input Class (except “GetString”) and Output Class  -Operate Calculations in each gate  -Preparing for Phase II and Main Design decisions: Toolbars and Modes  -Save Circuit  -Load Circuit (including all the new Constructors for each Component)  -Generate Truth Table |
| Ahmed Mohamed Mohamed Abdulsalam | 1190567 | -Connect and some of its Validations  -Delete Component  -Cut, Copy, and Paste Component  -Validate the circuit  -Probe Circuit Action |